

THIS OPINION WAS NOT WRITTEN FOR PUBLICATION

The opinion in support of the decision being entered today (1) was not written for publication in a law journal and (2) is not binding precedent of the Board.

Paper No. 24

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte NG WEE HUAT

Appeal No.1996-2956
Application 08/152,192

HEARD: MARCH 9, 2000

Before HAIRSTON, FLEMING, and DIXON, **Administrative Patent Judges.**

FLEMING, **Administrative Patent Judge.**

DECISION ON APPEAL

This is a decision on appeal from the final rejection of claims 27 through 34, all of the claims pending in the present application. Claims 1 through 26 have been canceled.

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The invention relates to a testing and finishing system for integrated circuit package units (ICPUs). In particular, Appellant discloses on page 2 of the specification that the present invention has integrated all individual operations into one assembly linking all the equipment and stations together forming an auto-test and finishing system. A copy of independent claim 27 is attached to this decision.

The Examiner relies on the following references:

Wilkin et al. (Wilkin)	3,842,957	Oct. 22, 1974
Swapp et al. (Swapp)	4,776,747	Oct. 11, 1988
Takemoto et al. (Takemoto)	4,850,103	July 25, 1989
Pearson	4,878,801	Nov. 7, 1989
Nara 1990	4,969,199	Nov. 6,
Yonemura (Japanese Patent)	58-18930	Jan. 3, 1983
Kodama (Japanese Patent)	60-161629	Aug. 23, 1985
Yabe 1985 (Japanese Patent)	60-153133	Aug. 12,
Noguchi (Japanese Patent)	61-30041	Feb. 12, 1986
Fukui (Japanese Patent)	62-86832	Apr. 21, 1987
Matsunaga (Japanese Patent)	63-257250	Oct. 25, 1988

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Tomita
(Japanese Patent)

1-181551

July 19, 1989

Claims 27 through 31, 33 and 34 stand rejected under 35 U.S.C. § 103 as being unpatentable over Appellant's admitted prior art, Swapp, Kodama, Fukui, Tomita, Wilkin, Takemoto, Yonemura, Nara, Noguchi and Pearson.

Claim 32 stands rejected under 35 U.S.C. § 103 as being unpatentable over the combination of Appellant's admitted prior art, Swapp, Kodama, Fukui, Tomita, Wilkin, Takemoto, Yonemura, Nara, Noguchi and Pearson, and further in view of Yabe and Matsunaga.

Rather than reiterate the arguments of Appellant and the Examiner, reference is made to the briefs¹ and the answer for the respective details thereof.

OPINION

We will not sustain the rejection of claims 27 through 34 under 35 U.S.C. § 103.

¹ Appellant filed an appeal brief on June 23, 1995. Appellant filed a reply brief on October 23, 1995. The Examiner mailed a communication on February 6, 1996 stating that the reply brief has been entered and considered but no further response by the Examiner is deemed necessary.

The Examiner has failed to set forth a ***prima facie*** case. It is the burden of the Examiner to establish why one having ordinary skill in the art would have been led to the claimed invention by the express teachings or suggestions found in the prior art, or by implications contained in such teachings or suggestions. ***In re Sernaker***, 702 F.2d 989, 995, 217 USPQ 1, 6 (Fed. Cir. 1983). "Additionally, when determining obviousness, the claimed invention should be considered as a whole; there is no legally recognizable 'heart' of the invention." ***Para-Ordnance Mfg. v. SGS Importers Int'l, Inc.***, 73 F.3d 1085, 1087, 37 USPQ2d 1237, 1239 (Fed. Cir. 1995), ***cert. denied***, 519 U.S. 822 (1996), ***citing W. L. Gore & Assocs., Inc. v. Garlock, Inc.***, 721 F.2d 1540, 1548, 220 USPQ 303, 309 (Fed. Cir. 1983), ***cert. denied***, 469 U.S. 851 (1984).

On pages 16-24 of the brief, Appellant argues that the Examiner has failed to recognize that the prior art does not teach automatic transportation of unenclosed ICPUs from one treatment or test station to another. Appellant further argues that the Examiner has failed to recognize that the prior art does not teach the integration of treatment and test stations for testing, marking, sorting, and packing ICPUs of

different categories without the need to package and repackage ICPUs before separate individual process operations are performed. On page 2

of the reply brief, Appellant further argues that the prior art does not teach the continuous linking of process stations and the automatic movement of unenclosed ICPUs from one process station to another process station. On page 23 of the brief, Appellant further argues that there must be some logical reason for combining the prior art and formulating a rejection other than the hindsight gleaned from the invention itself. Appellant argues that it appears that the Examiner's compilation of prior art is not based upon any logical connection of such art, but upon an attempt to fashion a theory extracted from Appellant's teachings.

On page 9 of the answer, the Examiner responds to Appellant's argument stating that it has been recognized that any judgment on obviousness is, in a sense, necessarily a reconstruction based upon hindsight reasoning. The Examiner further states that so long as the Examiner's rejection takes

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into account only the knowledge which was within the level of ordinary skill at the time the claimed invention was conceived, and so long as the rejection does not include knowledge gleaned only from Appellant's disclosure, such a reconstruction is proper.

The Federal Circuit states that "[t]he mere fact that the prior art may be modified in the manner suggested by the Examiner does not make the modification obvious unless the prior art suggested the desirability of the modification." **In re Fritch**, 972 F.2d 1260, 1266 n.14, 23 USPQ2d 1780, 1783-84 n.14 (Fed. Cir. 1992), **citing In re Gordon**, 733 F.2d 900, 902, 221 USPQ 1125, 1127 (Fed. Cir. 1984). It is further established that "[s]uch a suggestion may come from the nature of the problem to be solved, leading inventors to look to references relating to possible solutions to that problem." **Pro-Mold & Tool Co. v. Great Lakes Plastics, Inc.**, 75 F.3d 1568, 1573, 37 USPQ2d 1626, 1630 (Fed. Cir. 1996), **citing In re Rinehart**, 531 F.2d 1048, 1054, 189 USPQ 143, 149 (CCPA 1976)(considering the problem to be solved in a determination of obviousness). The Federal Circuit reasons in **Para-Ordnance Mfg. Inc. v. SGS Importers Int'l Inc.**, 73 F.3d 1085, 1088-89,

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37 USPQ2d 1237, 1239-40 (Fed. Cir. 1995), ***cert. denied***, 519
U.S. 822 (1996), that for the determination of obviousness,
the court must answer whether one of ordinary skill in the art
who sets out to solve the problem and who had before him in
his workshop the prior art, would have been reasonably
expected to use the solution that is claimed by the
Appellants. However, "[o]bviousness may not be established
using hindsight or

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in view of the teachings or suggestions of the invention."

Para-Ordnance Mfg. v. SGS Importers Int'l, 73 F.3d at 1087, 37 USPQ2d at 1239, **citing W.L. Gore & Assocs., Inc. v. Garlock, Inc.**, 721 F.2d at 1551, 1553, 220 USPQ at 311, 312-13. In addition, our reviewing court requires the PTO to make specific findings on a suggestion to combine prior art references. **In re Dembiczak**, 175 F.3d 994, 1000-01, 50 USPQ2d 1614, 1617-19 (Fed. Cir. 1999).

Upon our review of the references cited by the Examiner, we fail to find that the Examiner has made specific findings on a suggestion to combine these prior art references. In particular, we fail to find that the Examiner has shown that the prior art suggests automating transportation of unenclosed ICPUs from one treatment or test station to another station. In addition, the Examiner has failed to show that the prior art teaches or suggests the integration of treatment and test stations for testing, marking, sorting and packing ICPUs of different categories without the need to package and repackage ICPUs before separate individual process operations are performed.

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In view of the foregoing, we will not sustain the
rejection of claims 27 through 34 under 35 U.S.C. § 103.
Accordingly, the Examiner's decision is reversed.

REVERSED

KENNETH W. HAIRSTON)	
Administrative Patent Judge)	
)	
)	
)	BOARD OF PATENT
MICHAEL R. FLEMING)	
Administrative Patent Judge)	APPEALS AND
)	
)	INTERFERENCES
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JOSEPH L. DIXON)	
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APPENDIX

27. A method of testing, marking, sorting and packing different classification of integrated circuit package units (ICPUs) that are initially enclosed in carrier tubes comprising,

a) automatically positioning carrier tubes containing ICPUs in a position that locates the ICPUs in a dead bug orientation,

b) automatically moving the carrier tubes with the ICPUs in the previously positioned dead bug orientation to a conditioning station,

c) automatically unloading the ICPUs from the carrier tubes at the conditioning station in the dead bug orientation such that the ICPUs are unenclosed, and automatically conditioning the individual, unenclosed ICPUs with heat,

d) automatically transporting the conditioned ICPUs, while unenclosed and in the dead bug orientation, from the conditioning station to an environmental test station and automatically testing the electrical parameters of the conditioned ICPUs at the environmental test station while the ICPUs are in the dead bug orientation,

e) automatically cooling the conditioned and unenclosed ICPUs while the ICPUs are in the dead bug orientation and automatically transporting the cooled ICPUs, while the ICPUs are unenclosed and in the dead bug orientation, from the environmental test station to an ambient temperature test station,

f) automatically testing the cooled ICPUs at the ambient temperature test station for quality assurance while the ICPUs are unenclosed and in the dead bug orientation and thereafter automatically transporting the quality tested ICPUs, while unenclosed and in the dead bug orientation, from the ambient temperature test station to an orientation station,

g) automatically orienting the quality tested ICPUs at the orientation station while the ICPUs are unenclosed, from the dead bug orientation to a live bug orientation and automatically transporting the ICPUs while unenclosed and in the live bug orientation from the orientation station to a degreasing station,

h) automatically degreasing the ICPUs at the degreasing station while the ICPUs are unenclosed and in the live bug orientation and automatically transporting the degreased ICPUs, while the ICPUs are unenclosed and in the live bug orientation, from the degreasing station to a marking station,

i) providing a set of markers at the marking station, such that each marker in the set has different classification indicia corresponding to each different classification of the ICPUs and automatically marking the degreased ICPUs at the marking station while the ICPUs are unenclosed and in the live bug orientation, with a classification indicia that corresponds to the classification of the ICPU, and automatically transporting the marked ICPUs, while the ICPUs are unenclosed and in the live bug orientation, from the marking station to an ultraviolet station,

j) automatically heating the marked ICPUs at the ultraviolet station while the ICPUs are unenclosed and in the live bug orientation, using an ultraviolet source, and automatically transporting the heated ICPUs, while the ICPUs are unenclosed and in the live bug orientation, from the ultraviolet station to a lead straightening station,

k) automatically scanning all the ICPUs at the lead straightening station while the ICPUs are unenclosed and in the live bug orientation, for any bent leads and automatically straightening any bent leads of the ICPUs while the ICPUs are in the live bug orientation, and automatically transporting the ICPUs, while the ICPUs are unenclosed and in the live bug orientation, from the lead straightening station to a binning, buttoning and packing station,

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l) at the binning, buttoning and packing station, automatically segregating ICPUs of common classification while the ICPUs are unenclosed and automatically loading the ICPUs of common classification into empty tubes that are buttoned at one end and automatically buttoning the other end of the tubes when they are loaded with ICPUs of common classification, and

m) linking the conditioning station, the environmental test station, the ambient temperature test station, the orientation station, the degreasing station, the marking station, the ultraviolet station, the lead straightening station and the binning, buttoning and packing station together in a continuous cooperative assembly to permit the unenclosed ICPUs to be transported automatically from station to station and integrating all individual operations to form a completely integrated auto testing and finishing system that enables the ICPUs to be automatically transported, while unenclosed, from station to station such that the automated linking of stations eliminates manual loading and unloading of ICPUs at each station.